



# UNITED STATES PATENT AND TRADEMARK OFFICE

11A

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/883,062

06/15/2001

Jan Medved

81862.P219

1703

7590

07/24/2006

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Seventh Floor

12400 Wilshire Boulevard

Los Angeles, CA 90025-1026

EXAMINER

MERED, HABTE

ART UNIT

PAPER NUMBER

2616

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/883,062

Applicant(s)

MEDVED ET AL

Examiner

Habte Mered

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 March 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-27 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-27 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 15 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. The amendment filed on 3/23/2006 has been entered and fully considered.

Claims 1-27 are pending.

#### ***Allowable Subject Matter***

2. The indicated allowability of claims 5-10, 12-13, 16, and 24-26 are withdrawn in view of the newly discovered reference(s) to Cisneros et al (US 5, 166, 926).

Rejections based on the newly cited reference(s) follow.

#### ***Claim Objections***

3. **Claims 19 and 27** are objected to because of the following informalities: The phrase "machine readable" needs to be replaced with "computer readable". Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. **Claims 24-26** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. **Claim 24** recites the limitation "... the shelves" in the third line of the claim. There is insufficient antecedent basis for this limitation in the claim.

7. **Claim 24** refers to port mapping table in line 5 of the claim and mapping table in the last line of the claim. It is not clear if the mapping table is the same as or different from the port mapping table. Further it is not clear how the mapping of the ingress

queues to the logical fabric port depends on the updated port mapping table as stated in lines 6-7 of the claim. Also it is not clear in this claim if port mapping table refers to the mapping of the ingress queues to the logical ports or the mapping of the logical to physical port.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. **Claims 1-7, 10, and 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros et al (US 5, 166, 926) in view of Rao et al (US 6, 674, 756) and Chapman et al (US 6, 628, 609), hereinafter referred to as Cisneros, Rao, and Chapman respectively.

*Cisneros teaches a logical to physical mapping mechanism to support atm cells routing in a large fault tolerant packet switch.*

10. Regarding **claims 1**, Cisneros discloses a method of switching fabric port mapping (**See Figure 4, step 430**) comprising broadcasting fabric specific broadcast control cells to all ports attached to the switching fabric (**See Figure 3A, signal 337 going to all ports and also Column 18:8-12**) wherein the broadcasts control cells contain the current logical to\_physical\_port mappings based on which packets in the line ingress queues are to be forwarded by the switching fabric. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17. Cisneros teaches that the instruction from the switch**

**controller indicating the current logical to\_physical\_port mappings is broadcast and since Cisneros switch is an ATM switch all control signals are based on control/signaling cells as defined by the ATM Forum.)**

Cisneros fails to disclose a method of switching fabric port mapping comprising: associating line ingress queues with logical fabric ports.

*Chapman teaches a switch implemented as a router with a switch fabric capable of establishing logical pathways to interconnect a specific input port with a specific output port.*

Chapman discloses a method of switching fabric port mapping comprising: associating line ingress queues with logical fabric ports. **(See Figure 6, Table 602 and Columns 14:60-67 and 15:1-30)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate associating line ingress queues with logical fabric ports. The motivation being such an association of line ingress queues with logical fabric ports solves the classic Head Of Line problem. Given that physical port addresses change often due to card failures, a further motivation is that by associating the input queues with logical fabric ports as opposed to physical addresses of the port minimizes expensive changes in switch software.

Cisneros fails to teach a switch that has ports on shelves and uses a switching fabric port mapping.

*Rao teaches a multi-service network switch.*

Rao discloses a switch that has ports on shelves (**Column 22:11-16**) and ingress/egress queues (**See Figures 8 and 31-36 and Column 12:37-67**) and uses a switching fabric port mapping.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate a switch that has ports on shelves and uses a switching fabric port mapping. The motivation being use of having similar ports on a given shelf helps in providing service modularity and ease of implementation and also allows ability to add a local level maintenance controller over the ports/line cards on each shelf.

11. Regarding **claim 2**, Cisneros teaches a method wherein the logical to physical port mappings include the mapping of the ports that initiated the broadcasting. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17**)

Cisneros fails to teach a switch that has ports on shelves.

Rao discloses a switch that has ports on shelves (**Column 22:11-16**)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate a switch that has ports on shelves. The motivation being use of having similar ports on a given shelf helps in providing service modularity and ease of implementation and also allows ability to add a local level maintenance controller over the ports/line cards on each shelf.

12. Regarding **claim 3**, Cisneros discloses a method wherein the presence of a line card on a given fabric logical port is propagated to all other line cards in the system. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17**)

Art Unit: 2616

13. Regarding **claim 5**, Cisneros discloses a method, wherein the fabric control cell mechanism immediately broadcasts a change in the logical to physical port mappings upon the failure of an active line card. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17.)**

14. Regarding **claim 6**, Cisneros discloses a method wherein the fabric control cells mechanism periodically broadcasts the current logical to physical to logical-port mappings. **(See Column 14:26-43 Period diagnostics results in forcing the controller to send mappings as a result of detecting failure during the diagnostic period.)**

15. Regarding **claim 7**, Cisneros discloses a method wherein there are instances of multiple fabric control cell broadcasts ongoing. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17)**

16. Regarding **claim 10**, a method wherein the periodic broadcasts are made even when there is no card in a given slot. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17 and Column 14:26-43)**

17. Regarding **claim 20**, Cisneros discloses a switching fabric port mapping system comprising: a broadcast control mechanism which updates logical to physical port mappings; wherein packets in the line ingress queues are to be forwarded by the switching fabric based on the updated logical to physical mappings. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17)**

Cisneros fails to disclose a system of switching fabric port mapping comprising: associating each source line card with a plurality of line ingress queues. Chapman discloses a system of switching fabric port mapping comprising: associating each input port with a plurality of line ingress queues. **(See Figure 6, Table 602 and Columns 14:60-67 and 15:1-30)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' system to incorporate associating line ingress queues with each input port. The motivation being such an association of line ingress queues with input ports solves the classic Head Of Line problem. Given that physical port addresses change often due to card failures, a further motivation is that by associating the input queues with input ports as opposed to physical addresses of the port minimizes expensive changes in switch software.

Cisneros fails to disclose a multi-shelf switching fabric with source line cards and destination cards and each card having a port as well as the switch having a plurality of ingress/egress queues.

Rao discloses a multi-shelf switching fabric **(Column 22:11-16)** with source line cards and destination cards and each card having a port **(Figure 1 and Column 3:63-67 and Column 4:1-10, 12:60-67, 13:1-5)** as well as the switch having a plurality of ingress/egress queues **(Figure 36 and Column 30:48-56)**.



18. Regarding **claim 22**, Cisneros fails to disclose a system wherein a port mapping is executed in a multi-shelf switching environment.

Rao discloses a port mapping (**See Figure 31-36**) is executed in a multi-shelf switching environment (**Column 22:11-16**).

19. With respect to **claims 20 and 22**, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' system to incorporate a multi-shelf switch with source line cards and destination cards and each card having a port as well as the switch having a plurality of ingress/egress queues. The motivation being use of a multi-shelf arrangement having similar ports on a given shelf helps in providing service modularity and ease of implementation and also allows ability to add a local level maintenance controller over the ports/line cards on each shelf.

20. Regarding **claim 21**, Cisneros discloses a system further comprising a distributed broadcast mechanism to redirect traffic. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17**)

21. Regarding **claims 4 and 23**, Cisneros discloses a system wherein mapping tables are updated by a fabric control cell mechanism. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17. Cisneros teaches that the instruction from the switch controller indicating the current logical to\_physical\_port mappings is broadcast and since Cisneros**

Art Unit: 2616

**switch is an ATM switch all control signals are based on control/signaling cells as defined by the ATM Forum. Examiner takes Official Notice that ATM forum has already taught broadcast signaling/control cells and it is known in the art that these cells are used for network management which include specifying routing information.)**

22. **Claims 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros in view of Chapman and Rao as applied to claim 1 above, and further in view of Keates et al (US 6, 738, 828), hereinafter referred to as Keates.

*Keates teaches methods and apparatus for providing a name resolution protocol.*

23. Regarding **claim 8**, Cisneros teaches a method of broadcasting by a switch controller. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17)**

24. Regarding **claim 9**, Cisneros discloses a method, wherein periodically the control cells for all line card slots are broadcast. **(See Column 14:26-43)**

25. With respect to **claims 8 and 9**, Cisneros fails to teach shelf managers with broadcasting capability.

Keates teaches shelf managers **(See Figure 2C, element 50)** with broadcasting (i.e. multicasting) capability **(See Column 5:65-67 and Column 6:1-40. Further see that every network element including the shelf controller (i.e. shelf manager) has broadcasting (i.e. multicasting) capability as discussed in Column 4:48-67 and is further illustrated in Figure 6.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate a switch that has a shelf manager with a capability of broadcasting. The motivation being it allows the switch to distribute centralized control functions to a local level such as the shelves housing the line cards with port interfaces in order to increase overall processing speed because the shelf manager will be able to detect card failure and issue broadcast message containing corrective action faster than the centralized switch controller.

26. **Claims 11, 12, 15, 18, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros et al (US 5, 166, 926) in view of Chapman et al (US 6, 628, 609), hereinafter referred to as Cisneros and Chapman respectively.

27. Regarding **claims 11, 15, and 19**, Cisneros discloses a switching fabric port mapping apparatus (**Figure 2, element 290**) comprising: means and circuitry for broadcasting the-logical to physical port\_mappings based on which packets in the line ingress queues are to be forwarded by the switching fabric. (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17**)

28. With respect to **claims 11, 12, 15, and 19**, Cisneros fails to disclose a means for mapping-associating line ingress queues to logical fabric ports; and the apparatus wherein an output queue is associated with a logical destination port.

Chapman discloses a means for mapping-associating line ingress queues to logical fabric ports; and the apparatus (**Figure 3, element 308**) wherein an output

queue is associated with a logical destination port. **(See Figure 6, Table 602 and Columns 14:60-67 and 15:1-30)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' apparatus to incorporate a means for associating line ingress queues with logical fabric ports and wherein an output queue is associated with a logical destination port. The motivation being such an association of line ingress queues with logical fabric ports solves the classic Head Of Line problem. Given that physical port addresses change often due to card failures, a further motivation is that by associating the input queues with logical fabric ports as opposed to physical addresses of the port minimizes expensive changes in switch software.

29. Regarding **claim 18**, Cisneros discloses an apparatus, wherein there are instances of multiple control cell broadcasts ongoing. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17)**

30. **Claims 13 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros in view of Chapman as applied to claims 11 and 15 above respectively, and further in view of Nair et al (US Pub. No. 2002/0103921), hereinafter referred to as Nair.

The combination of Cisneros and Chapman teaches all aspects of the claimed invention as set forth in the rejection of claims 11 and 15 but does not disclose an apparatus, wherein the logical fabric ports are globally managed.

*Nair teaches method and system for routing broadband Internet traffic.*

Nair discloses an apparatus, wherein the logical fabric ports are globally managed. **(See Paragraph 91. The Global Interface Manager (Fig. 4, element 408) resides on the Master Management Card (Figure 4, element 160) and manages the logical ports at a global level.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' apparatus to incorporate a means for globally managing logical ports. The motivation being managing logical ports globally minimizes redundancy and conflicts that can arise from managing logical ports locally.

31. **Claims 14, 17, and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros in view of Chapman as applied to claims 11, 16, and 19 above respectively, and further in view of Rao et al (US 6, 674, 756), hereinafter referred to as Rao.

The combination of Cisneros and Chapman discloses an apparatus wherein the broadcasting is made to all ports on the switching fabric and the logical to physical port mappings include the mappings of the ports, which initiated the broadcasting. **(See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17)**

Cisneros fails to teach a switch that has ports on shelves.

Rao discloses a switch that has ports on shelves **(Column 22:11-16)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' apparatus to incorporate a switch that has ports on shelves. The motivation being use of having similar ports on a given shelf

helps in providing service modularity and ease of implementation and also allows ability to add a local level maintenance controller over the ports/line cards on each shelf.

32. **Claims 24-26** (as best understood in view of the 112 2<sup>nd</sup> paragraph rejection described above in items 4-7 of this Office Action) are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros et al (US 5, 166, 926) in view of Rao et al (US 6, 674, 756) and Chapman et al (US 6, 628, 609) and Keates et al (US 6, 738, 828), hereinafter referred to as Cisneros, Rao, Chapman, and Keates respectively.

33. Regarding **claim 24**, Cisneros discloses a method of switching fabric port mapping comprising: broadcasting fabric specific broadcast control cells; transmitting the broadcast control cells to each port; updating a port mapping table, wherein a logical to physical fabric port mapping (**See Figure 4, step 430**) is managed locally (**Figure 3A, element 310**) and it's mapping table updates are managed globally (**Figure 3A, element 290**). (**See Columns 17:59-67, 18:1-10, 48:48-67, 49:1-17. Cisneros teaches that the instruction from the switch controller indicating the current logical to\_physical\_port mappings is broadcast and since Cisneros switch is an ATM switch all control signals are based on control/signaling cells as defined by the ATM Forum.**)

Cisneros fails to disclose a method of switching fabric port mapping comprising: mapping line ingress queues to logical fabric ports. Chapman discloses a method of switching fabric port mapping comprising: mapping line ingress queues to logical fabric ports. (**See Figure 6, Table 602 and Columns 14:60-67 and 15:1-30**)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate mapping line ingress queues to logical fabric ports. The motivation being such an association of line ingress queues with logical fabric ports solves the classic Head Of Line problem. Given that physical port addresses change often due to card failures, a further motivation is that by associating the input queues with logical fabric ports as opposed to physical addresses of the port minimizes expensive changes in switch software.

Cisneros fails to disclose a switch with a shelf processor capable of terminating broadcast control cells.

Keates disclose a switch with a shelf processor (**i.e. Shelf Manager See Figure 2C, element 50**) capable of terminating broadcast control cells. (**Keates teaches shelf managers, See Figure 2C, element 50, with broadcasting (i.e. multicasting) capability (See Column 5:65-67 and Column 6:1-40.) The broadcasting/multicasting capability involves both terminating and originating multicast cells.**)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate a switch that has a shelf manager with a capability of broadcasting. The motivation being it allows the switch to distribute centralized control functions to a local level such as the shelves housing the line cards with

Art Unit: 2616

port interfaces in order to increase overall processing speed because the shelf manager will be able to detect card failure and issue broadcast message containing corrective action faster than the centralized switch controller.

Cisneros fails to teach a switch that has ports on shelves and uses a switching fabric port mapping.

Rao discloses a switch that has ports on shelves (**Column 22:11-16**) and ingress/egress queues (**See Figures 8 and 31-36 and Column 12:37-67**) and uses a switching fabric port mapping.

34. Regarding **claim 25**, Cisneros fails to disclose a method wherein the terminating is done by a processor located in a line card.

Rao discloses a method in a switch wherein the terminating is done by a processor located in a line card. (**See Figure 2 item 46 and also Columns 1:63-67, 4:1-10, and 10:6-26.**)

35. With respect to **claims 24 and 25**, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Cisneros' method to incorporate a switch that has ports on shelves where each port has a processor for terminating calls and also uses a switching fabric port mapping. The motivation being use of having similar ports on a given shelf helps in providing service modularity and ease of implementation and also allows ability to add a local level maintenance controller over the ports/line cards on each shelf.



Art Unit: 2616

36. Regarding **claim 26**, Cisneros discloses a method, wherein a fabric control mechanism supports either 1 for 1 sparing (**See Column 48:11-24**) or 1 for N (**See Column 47: 60-68**) sparing. (**See also Rao Column 23:1-12 and Figures 24-26**)

### ***Response to Arguments***

37. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

38. In item 21 of this Office Action, examiner took Official Notice to indicate that ATM forum has already taught broadcast signaling/control cells and it is known in the art that these cells are used for network management, which includes specifying routing information. Eram et al (US 6, 385, 200) teaches that this is the case in the abstract, in Columns 1:35-50, 2:22-32, 7:35-45, and 10:29-35.

### ***Conclusion***

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent (6, 888, 792) to Gronke discloses Physical Port Mapper.

US Patent (6, 798, 784) to Dove et al discloses a multi-shelved switch with Virtual Output Queuing


US Patent (6, 411, 599) to Blanc et al discloses using control cells for transmitting routing related information.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HM  
07-17-2006



HASSAN KIZOU  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600